ABSTRACT OF THE DISCLOSURE

Multiple data processing circuits may share a semiconductor memory circuit, such as double-data-rate synchronous dynamic random access memory (DDR-SDRAM). A data processing circuit (**202**-1 or **202**-2) ending control of a semiconductor memory circuit (**201**) supplies a clock enable signal and chip select signal at predetermined levels. A data processing circuit (**202**-2 or **202**-1) starting control of a semiconductor memory circuit (**201**) supplies a clock enable signal and chip select signal at the same predetermined levels, before the data processing circuit (**202**-1 or **202**-2) ending control stops supplying a clock enable signal and chip select signal. Therefore, a clock enable signal and chip select signal do not enter an undefined state, and malfunctions that could otherwise occur are prevented.